

**VIRTUAL MEMORY TRANSLATION CONTROL BY  
TLB PURGE MONITORING**

**ABSTRACT OF THE DISCLOSURE**

In a computer system, an architecture is disclosed for optimizing aspects of data movement operations by performing functions such as memory allocation and notification on hardware rather than software. In  
5 this environment, the claimed invention is a method and apparatus for ensuring the integrity of data movement operations from virtual memory. The invention monitors and detects Translation Lookaside Buffer ("TLB") purges, a hardware-based operation whose occurrence signals that virtual-  
to-physical mapping has changed. Responsive to detection of a TLB purge  
10 during the set up or execution of a data movement operation, the claimed invention aborts the operation, and then enqueues corresponding completion status information to notify processors of the event.

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